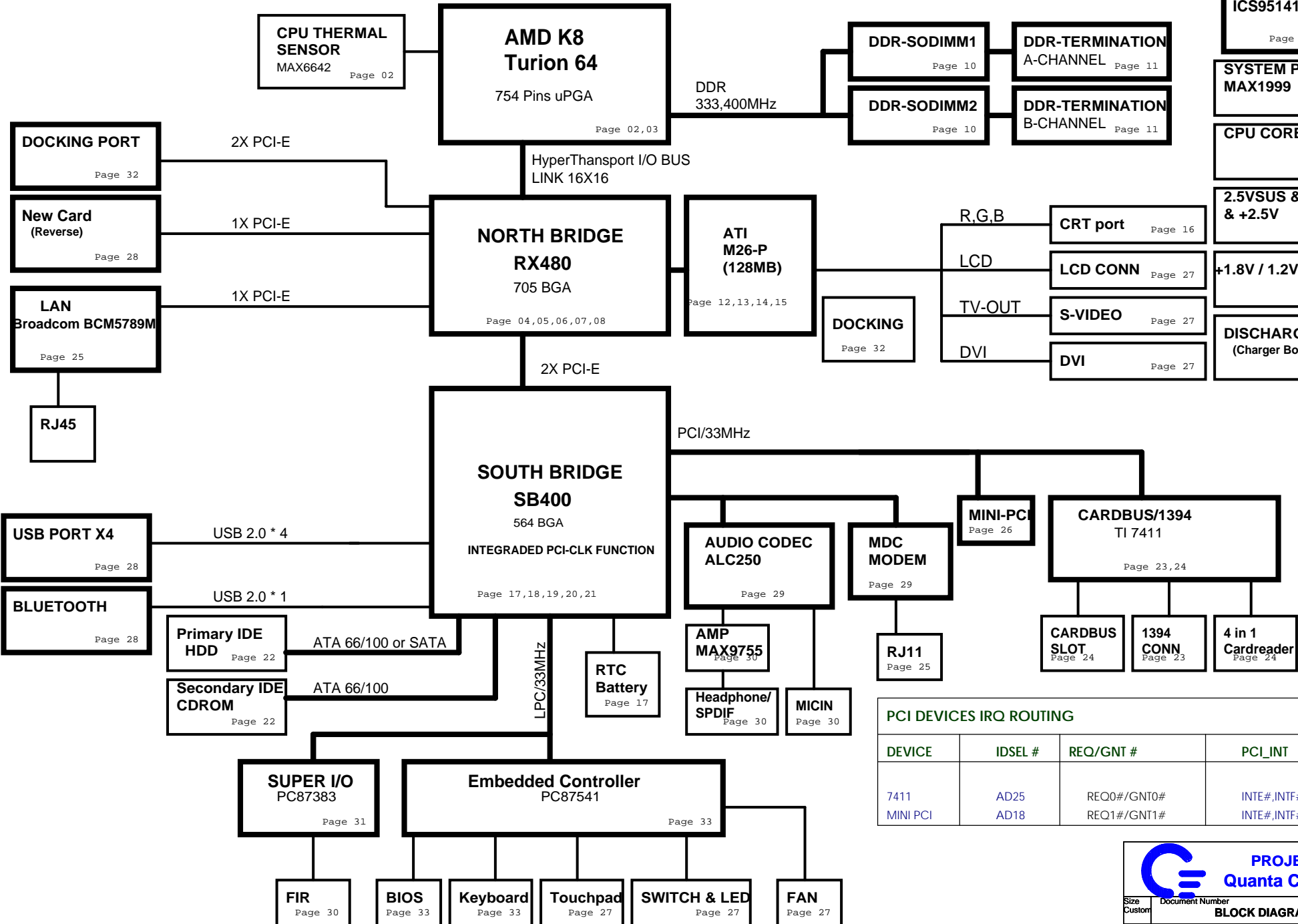
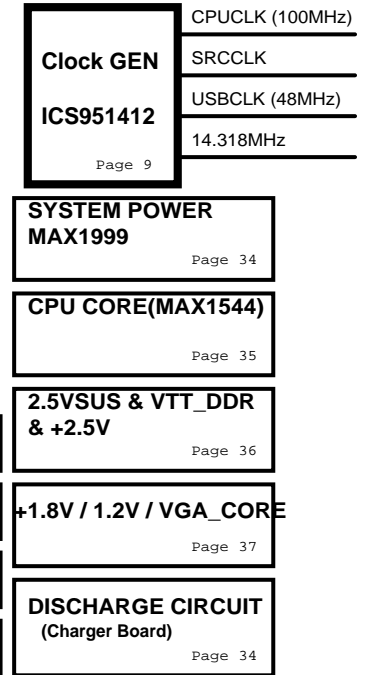


# ZF3 BLOCK DIAGRAM

## AMD K8/RX480/SB400

REV: G3A

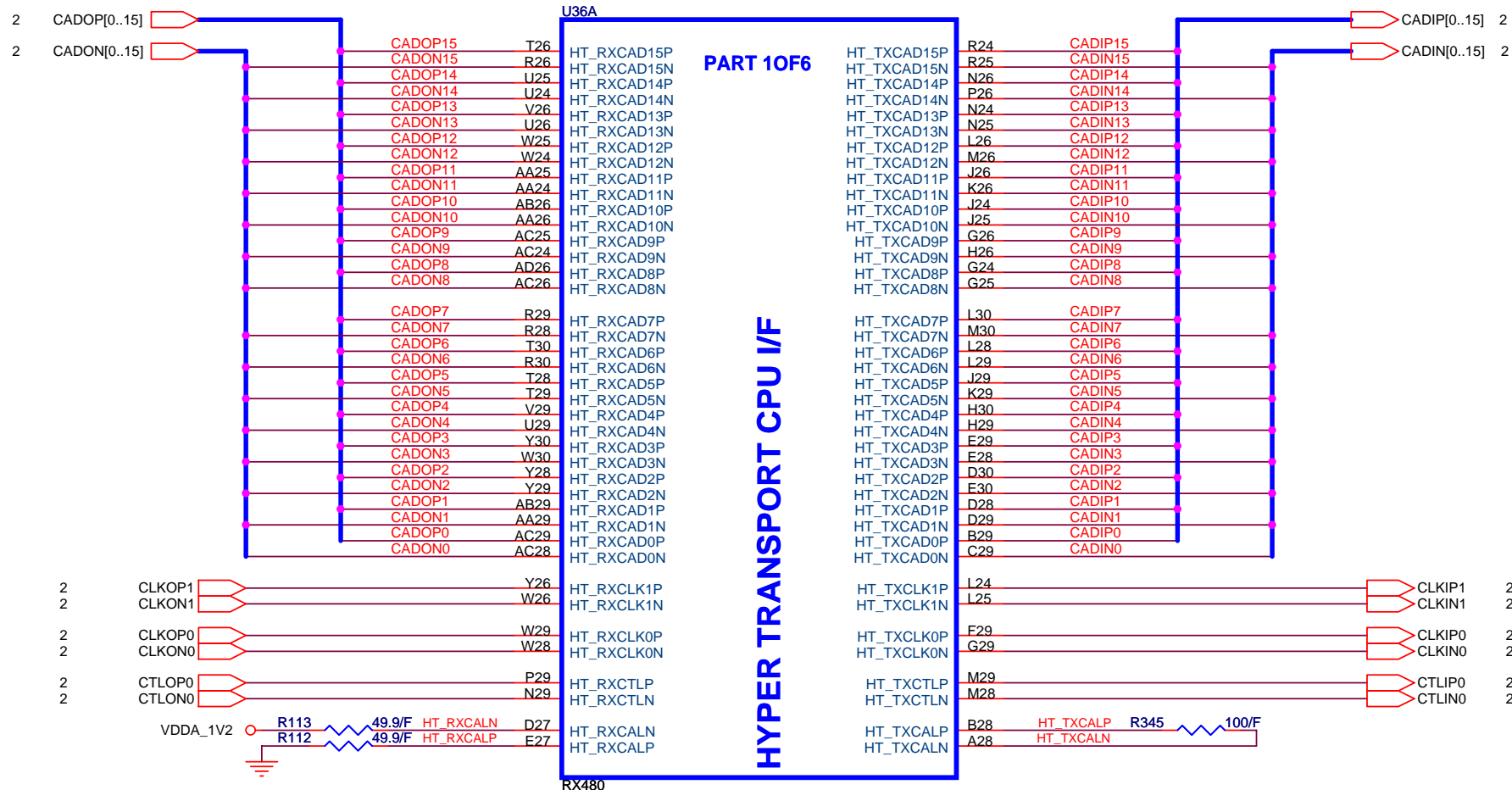


PCI DEVICES IRQ ROUTING			
DEVICE	IDSEL #	REQ/GNT #	PCI_INT
7411	AD25	REQ0#/GNT0#	INTE#,INTF#,INTH#
MINI PCI	AD18	REQ1#/GNT1#	INTE#,INTF#

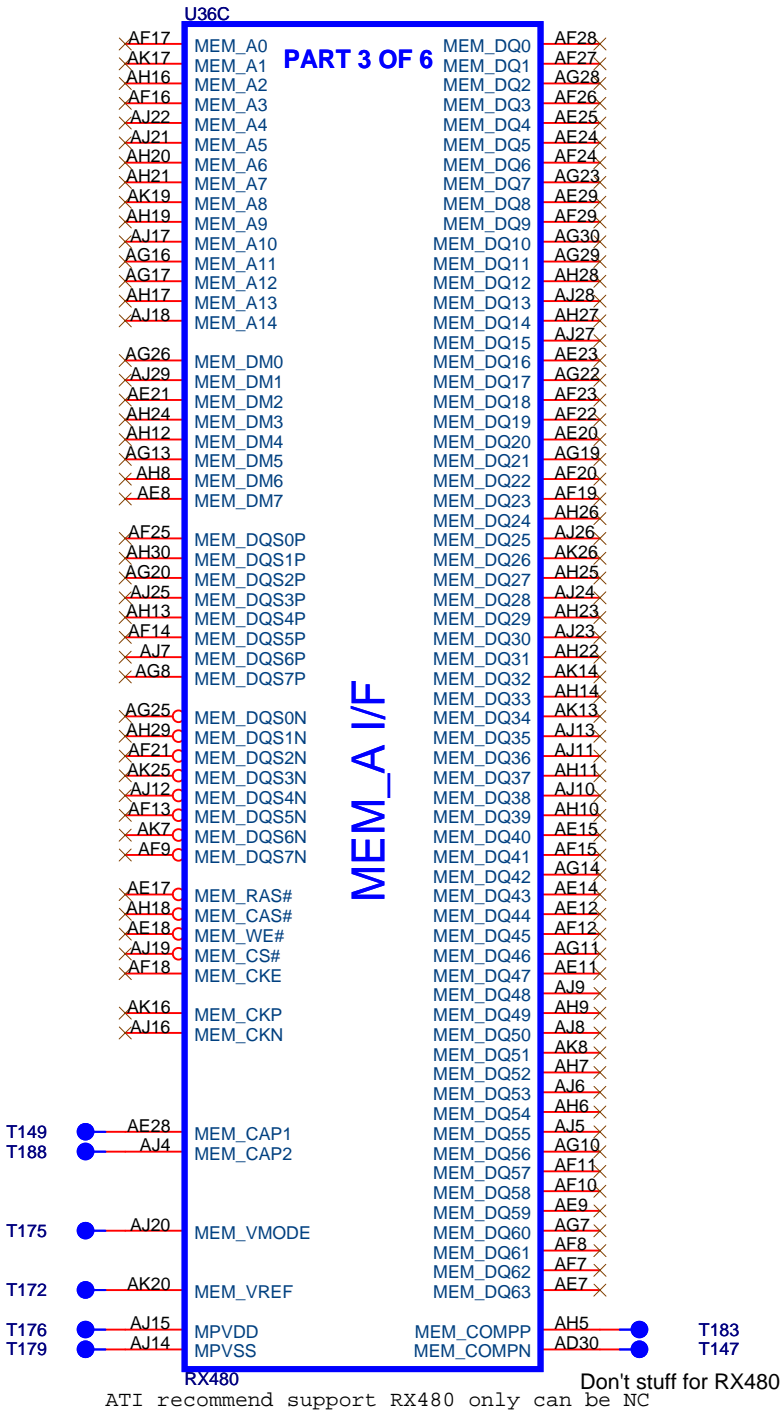





NB



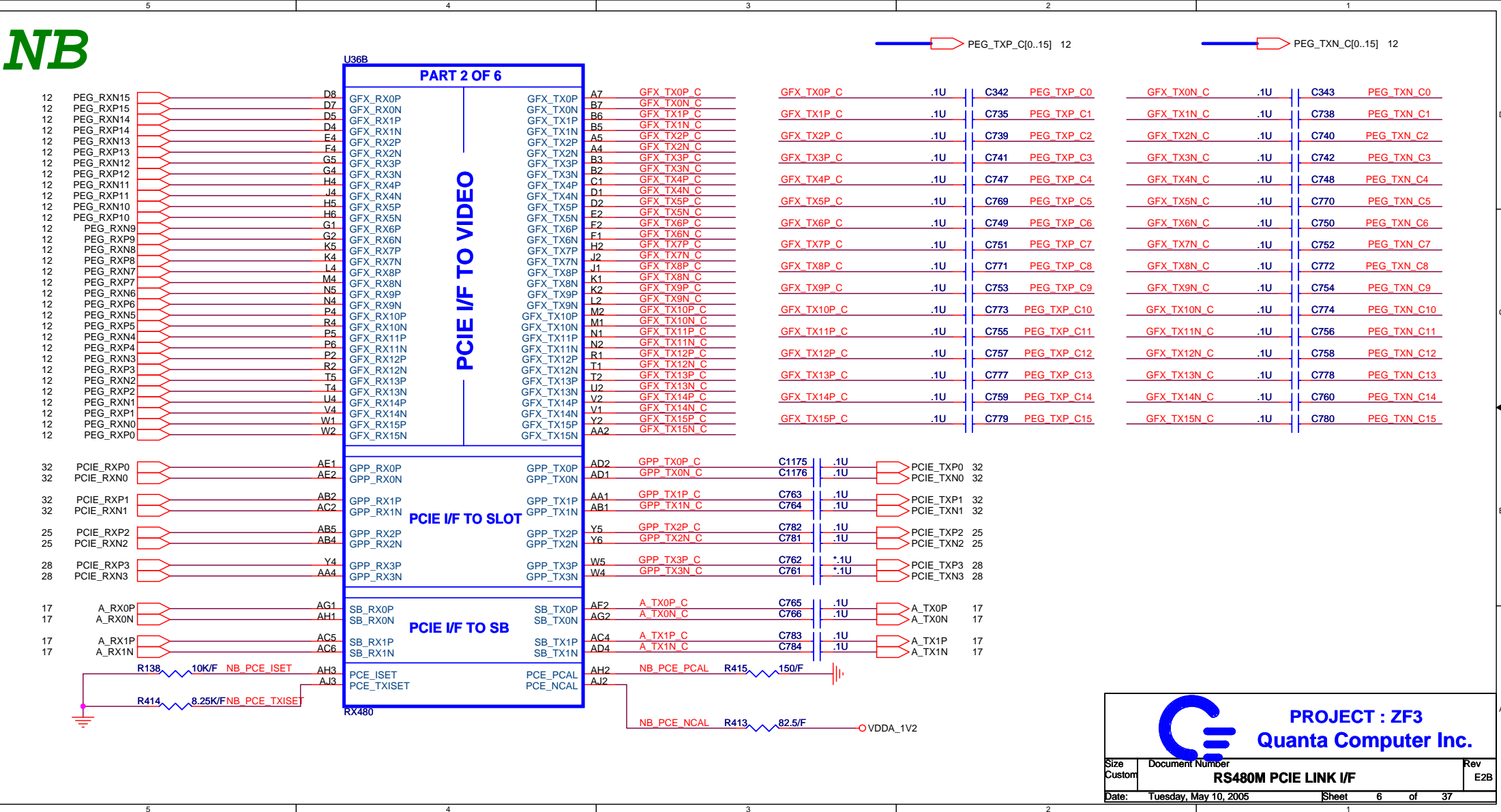
NB





**PROJECT : ZF3**  
**Quanta Computer Inc.**

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# NB

D

C

B

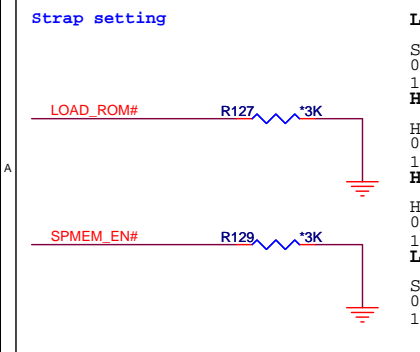
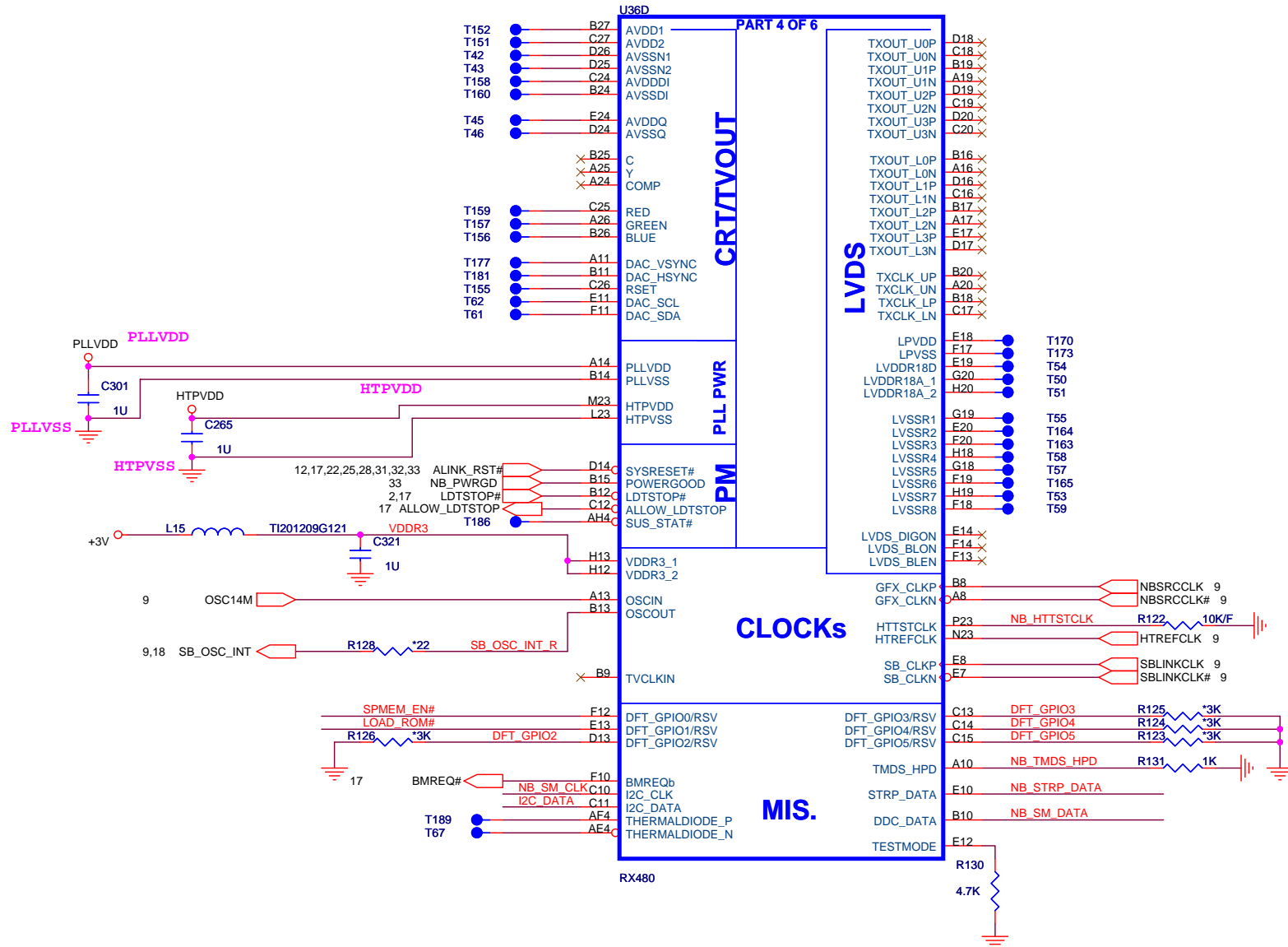
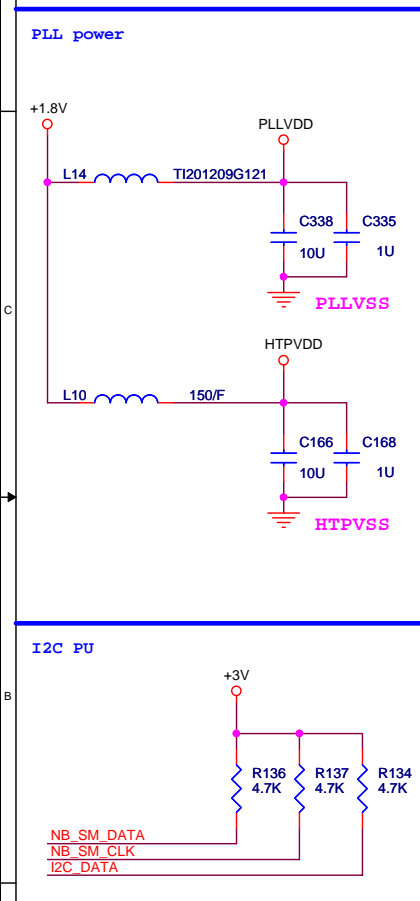
A

D

C

B

A



**LOAD\_MEM\_STRAPS#(DFT\_GPIO5)**

Selected loading of straps from MEM\_DQ pin for debug

0==>Capture MEM\_DQ pin for debug straps

1==>Use default value(Default)

**HT\_FREQ\_OVERRIDE(DFT\_GPIO[4:3])**

HT Frequency

00,01,10==>Reserve for test only

11==>200MHz(Default)

**HT\_WIDTH\_OVERRIDE(DFT\_GPIO2)**

HT link width

0==>Reserve for test only

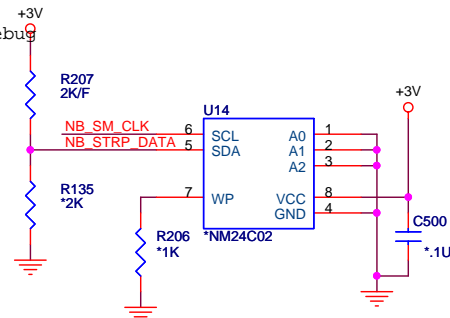
1==>8 bit link(Default)

**LOAD\_ROM\_STRAPS#(DFT\_GPIO1)**

Selected loads strap from EEPROM

0==>EEPROM strap

1==>Use default value(Default)



**PROJECT : ZF3**

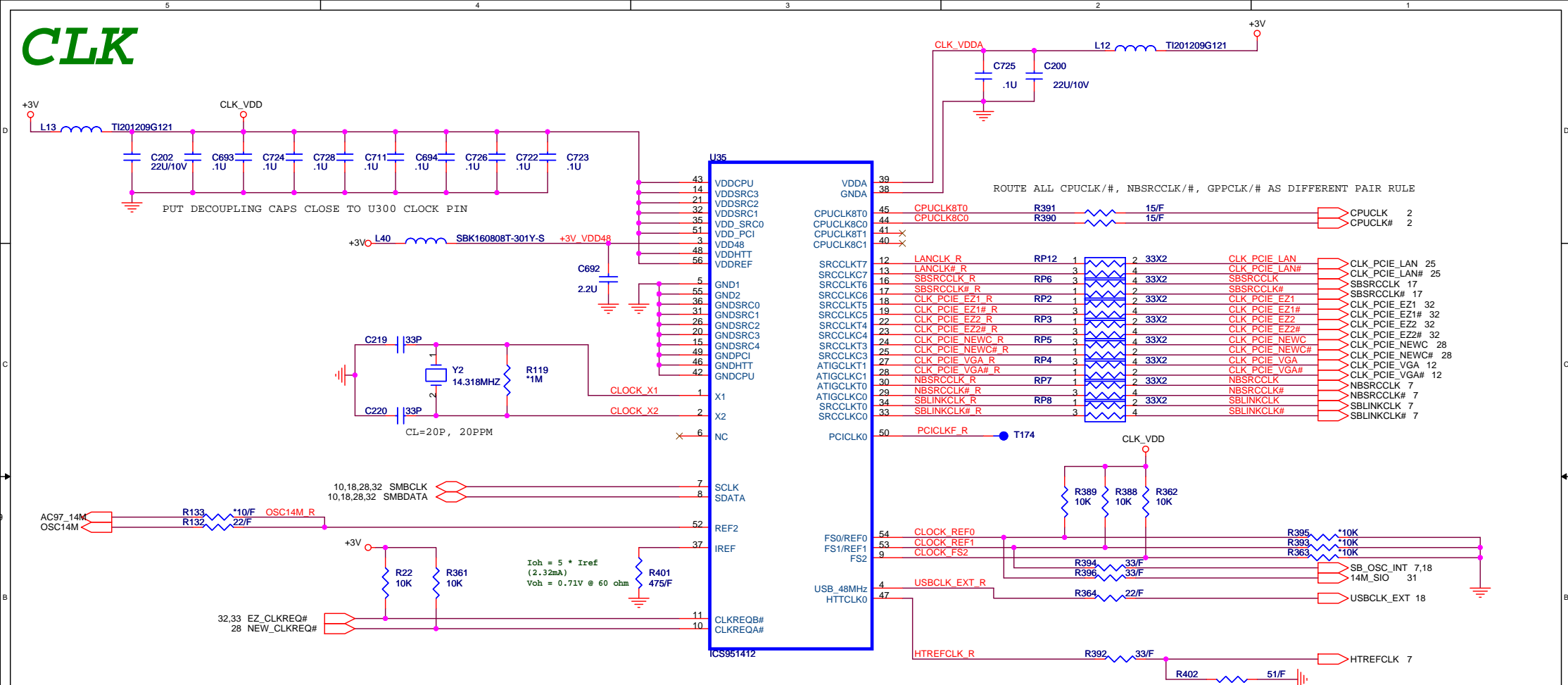
**Quanta Computer Inc.**

Size Custom Document Number **RS480M-VIDEO & CLKGEN** Rev E2B

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# CLK







# VGA

6 PEG\_TXP\_C[0..15]

6 PEG\_TXN\_C[0..15]

6 PEG\_RXP[0..15]

6 PEG\_RXN[0..15]

6 PEG\_RXP[0..15]

6 PEG\_RXN[0..15]

6 PEG\_RXP[0..15]

6 PEG\_RXN[0..15]

6 PEG\_RXP[0..15]

6 PEG\_RXN[0..15]

6 PEG\_RXP[0..15]

6 PEG\_RXN[0..15]

6 PEG\_RXP[0..15]

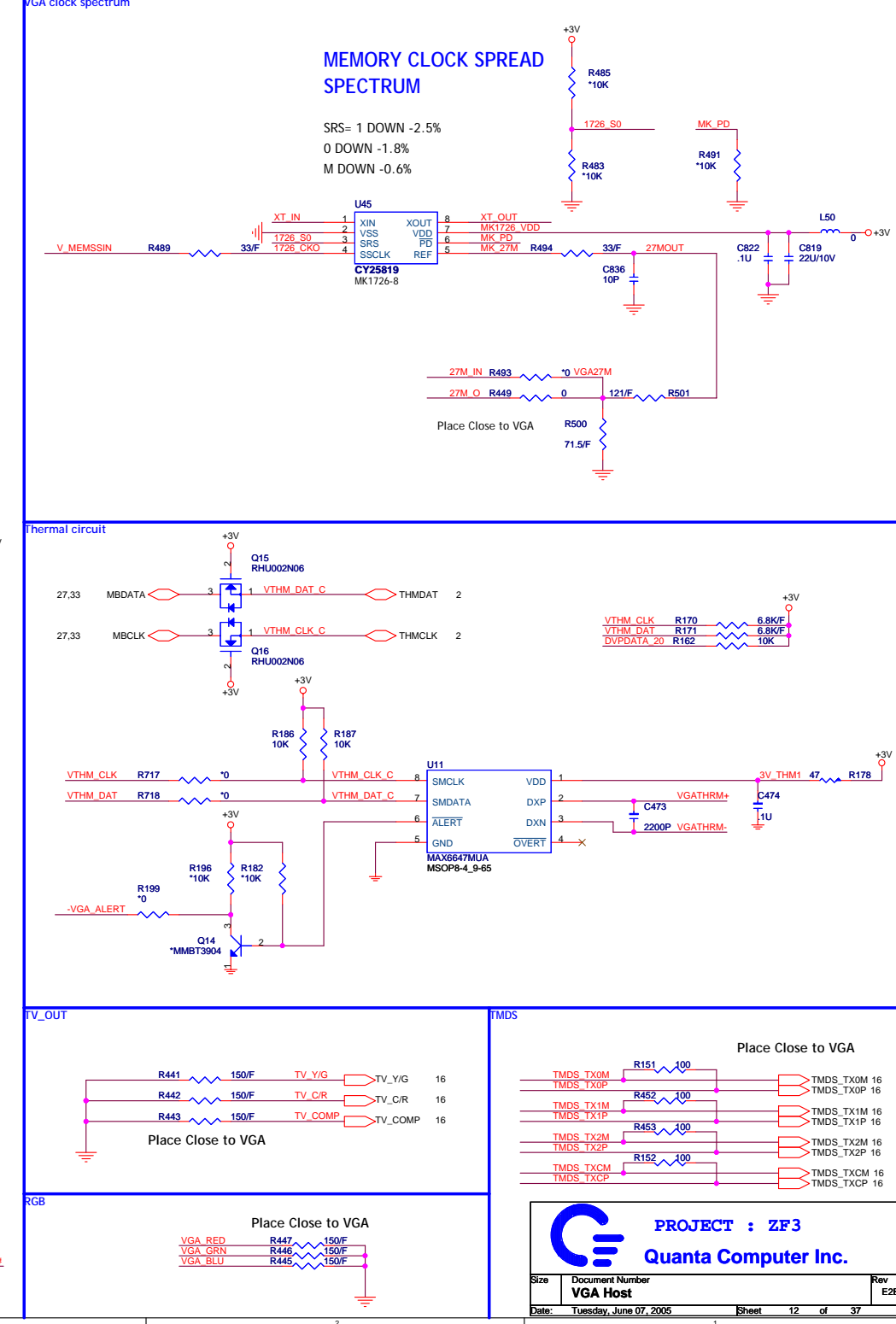
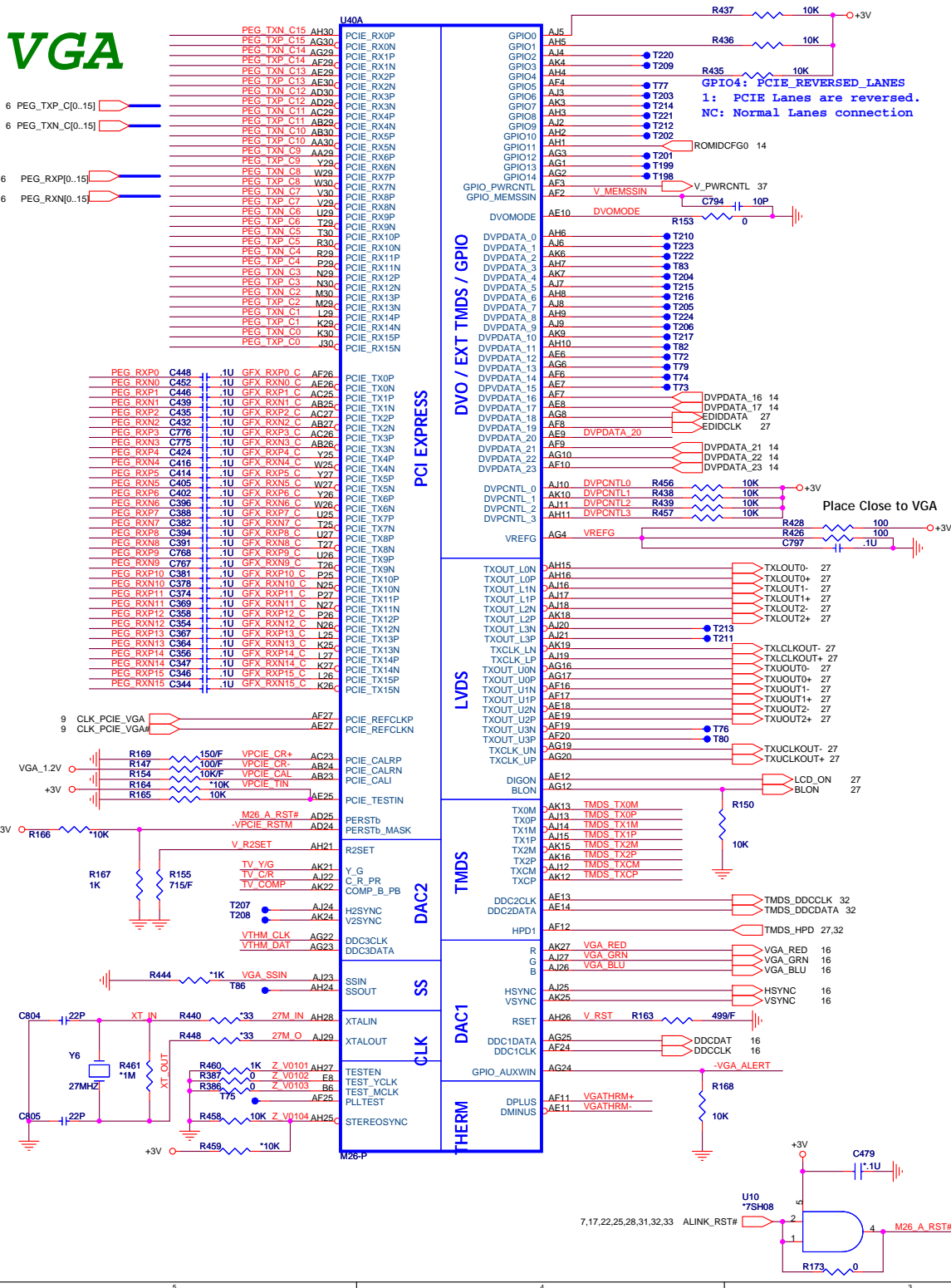
6 PEG\_RXN[0..15]

6 PEG\_RXP[0..15]

6 PEG\_RXN[0..15]

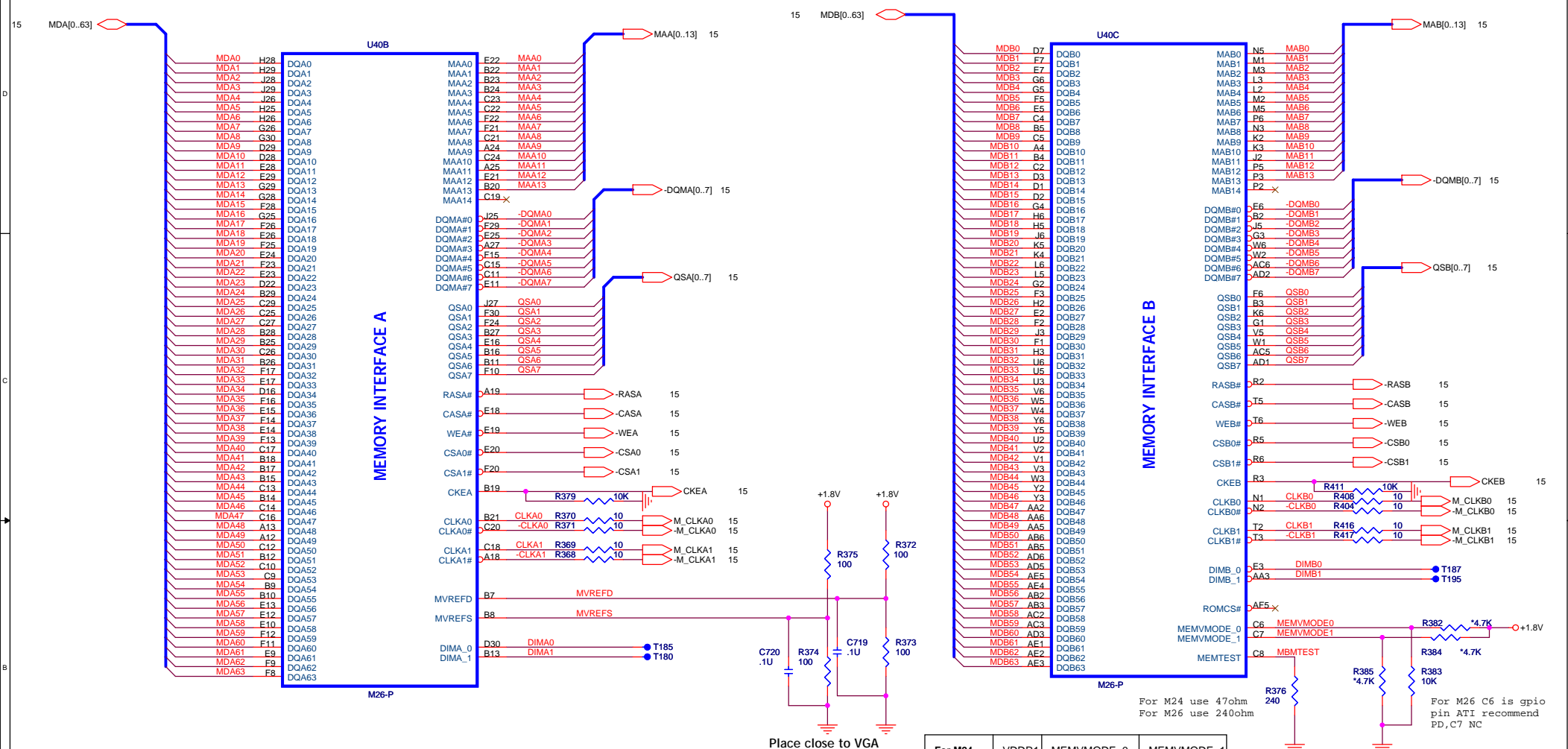
6 PEG\_RXP[0..15]

6 PEG\_RXN[0..15]





# VGA

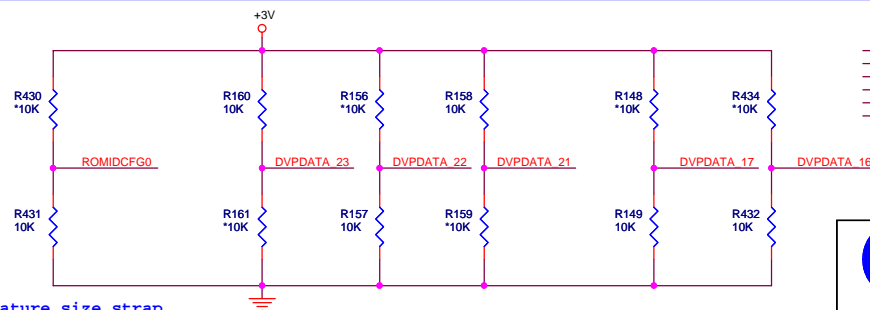


## STRAPS PIN

GPIO(9,13:11) INT P/D	ROMIDCFG	
	0x0x: No ROM, CHG_ID=0	0x1x: No Rom, CHG_ID=1
	1000: Parallel ROM, Chip ID'S from ROM	
	1000: Parallel ROM, Chip ID'S from ROM	
DVPDATA_21~23 MEM TYPE	DVPDATA_21: 0=4Mx32 1=8Mx32	
	DVPDATA_22: 0=128M 1=64M	
	DVPDATA_23: 0=Hynix 1=Samsung	

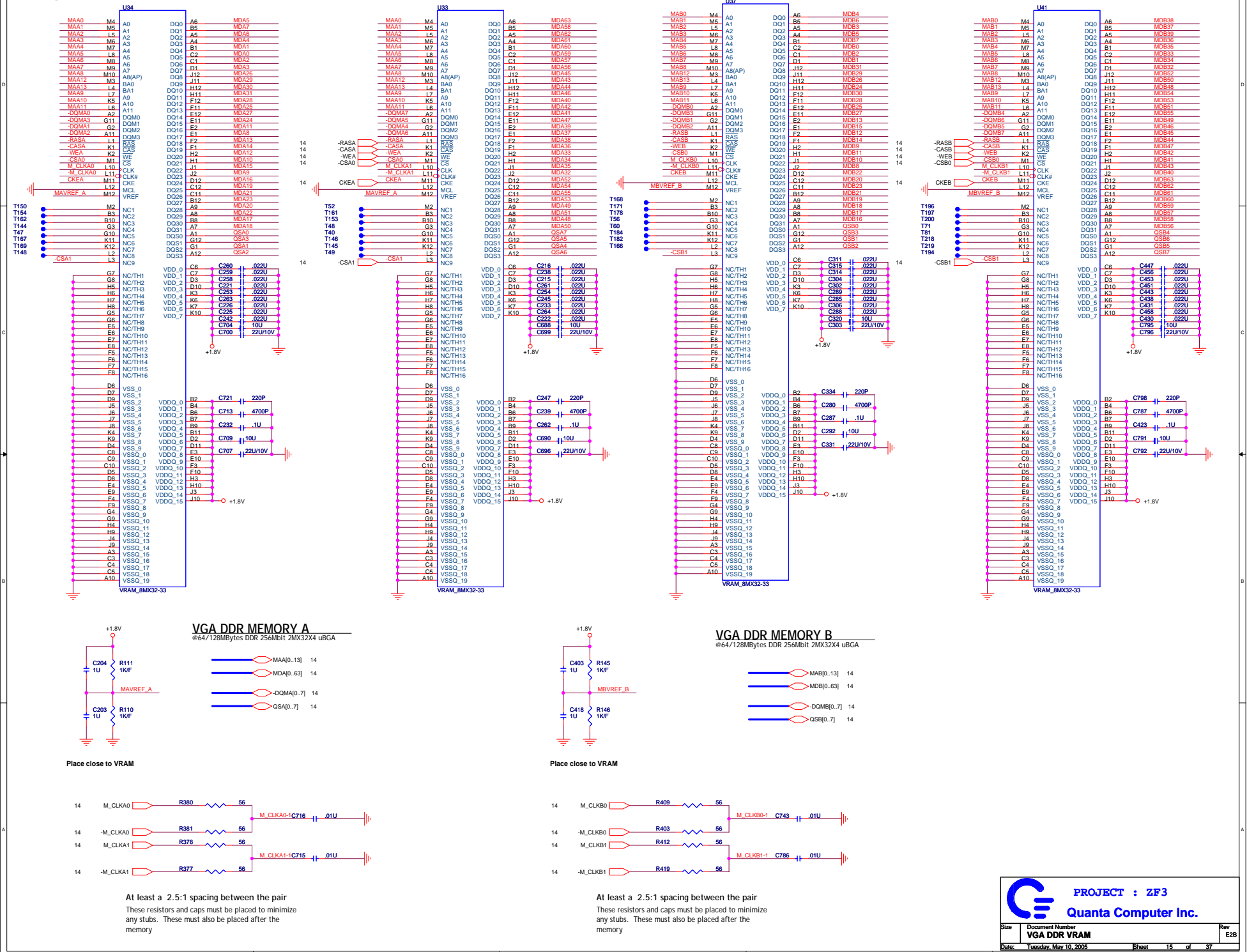
Default Samsung 128M

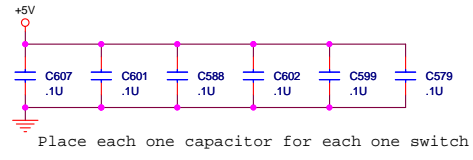
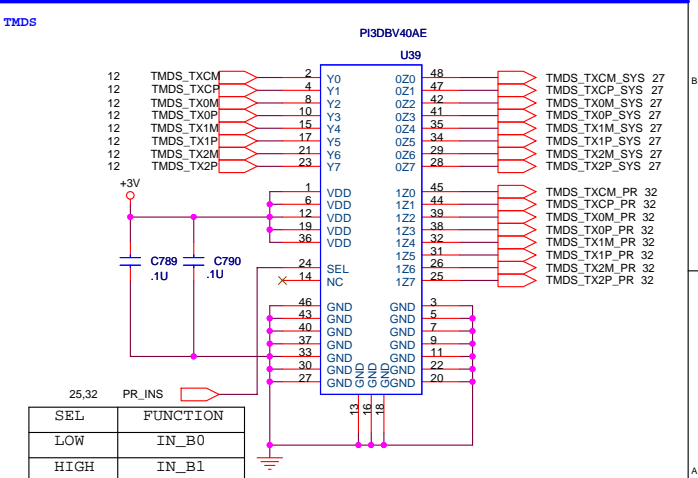
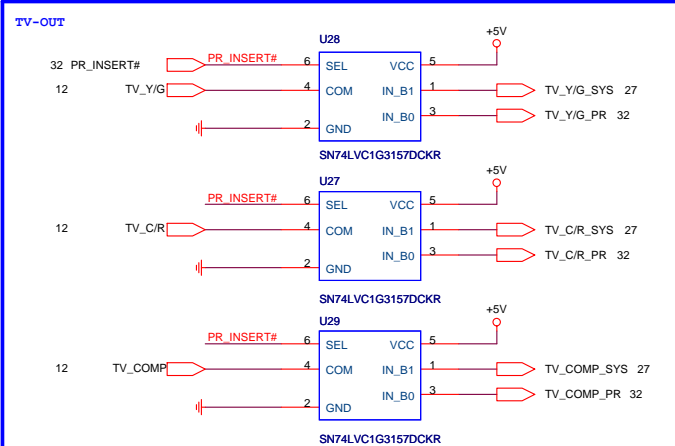
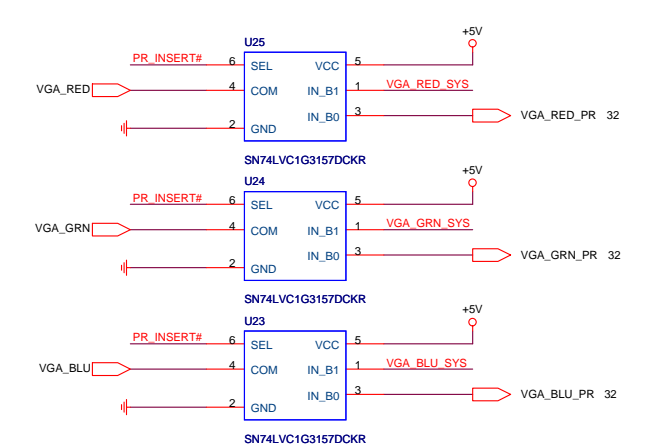
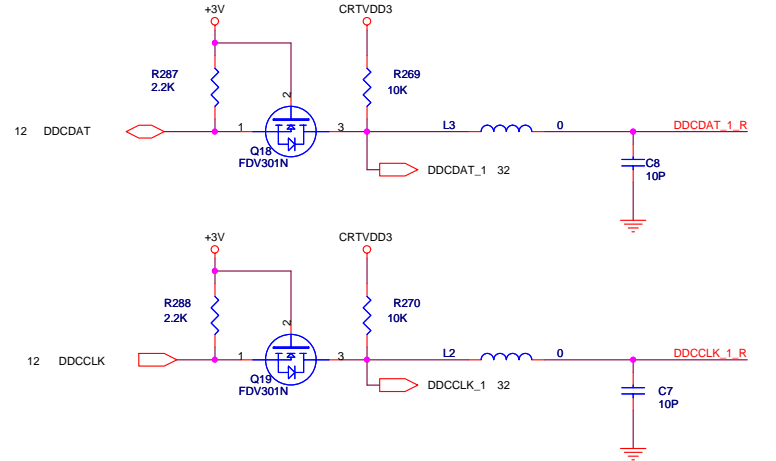
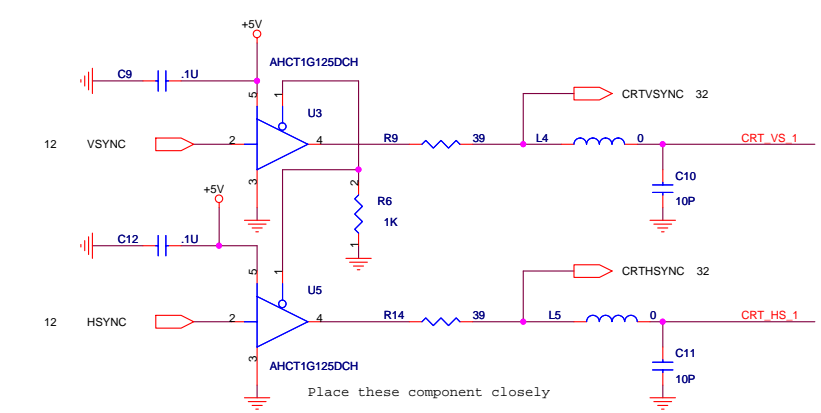
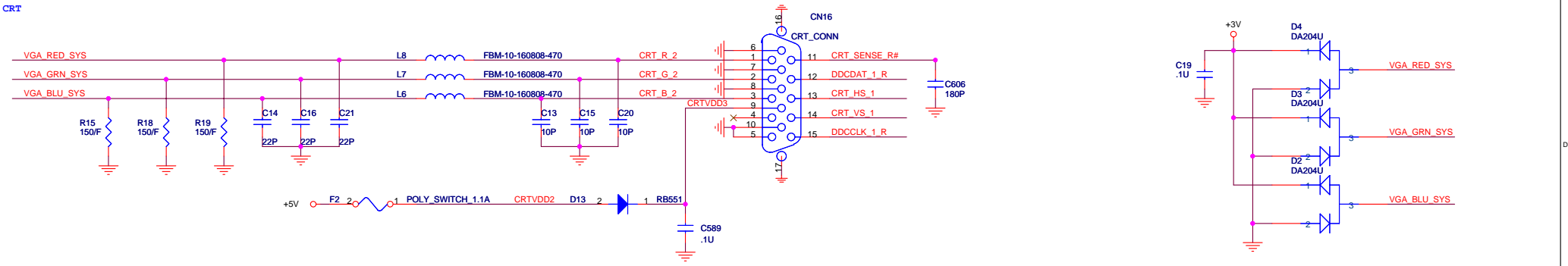
ROMID1 is aperture size strap  
0: 128M  
1: 256M



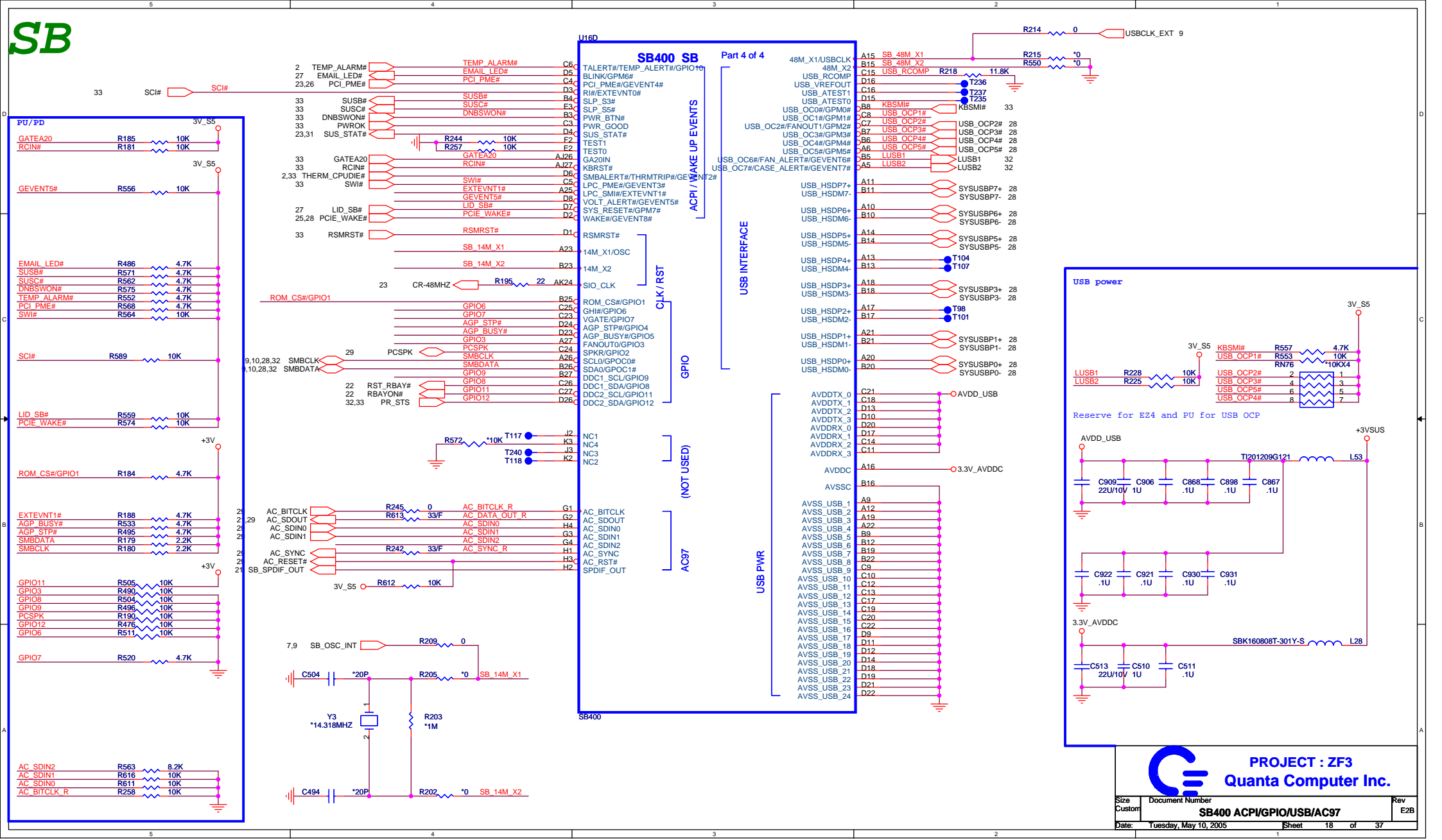
PROJECT : ZF3  
Quanta Computer Inc.

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	VGA MEM & Strapping	E2B
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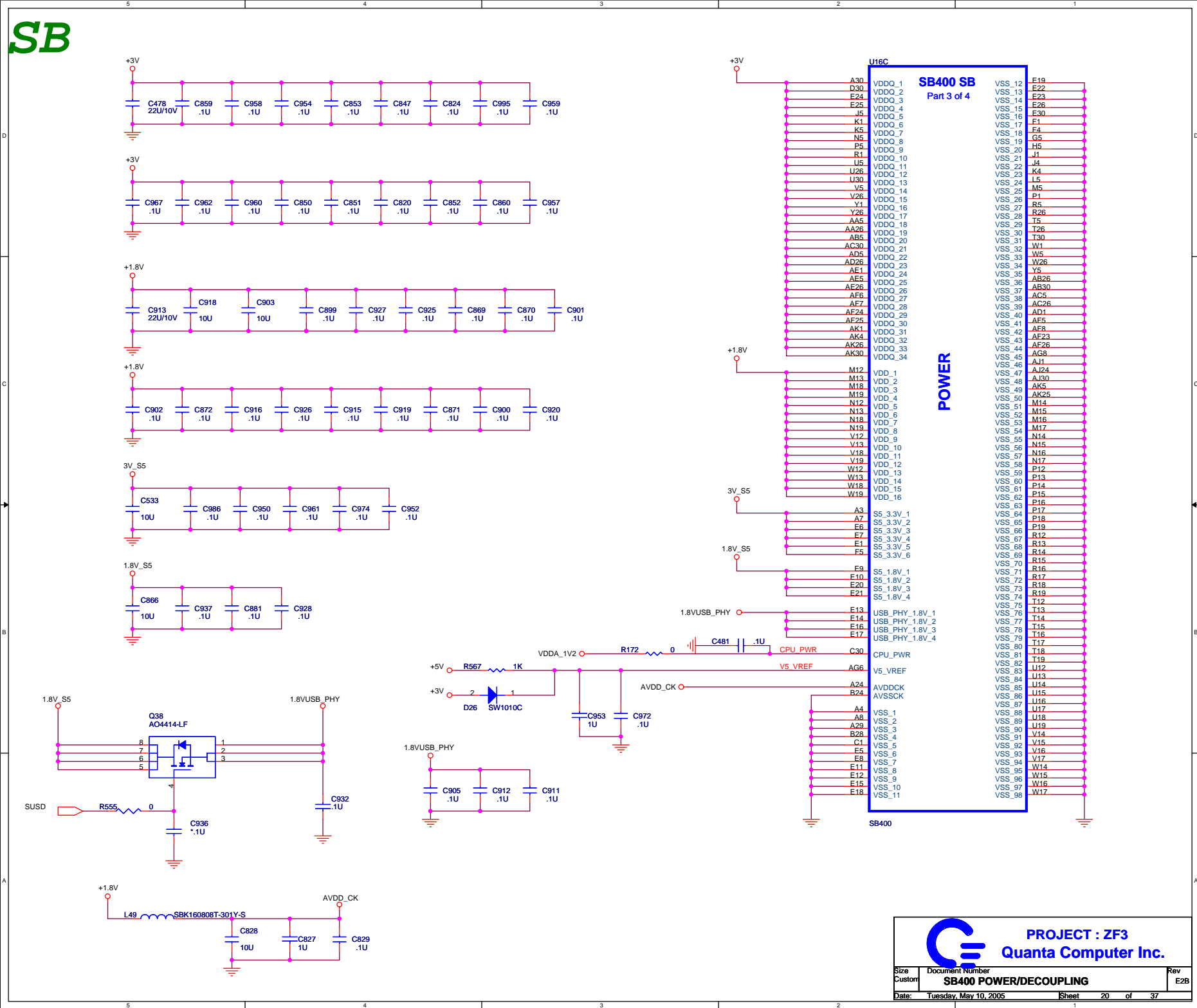


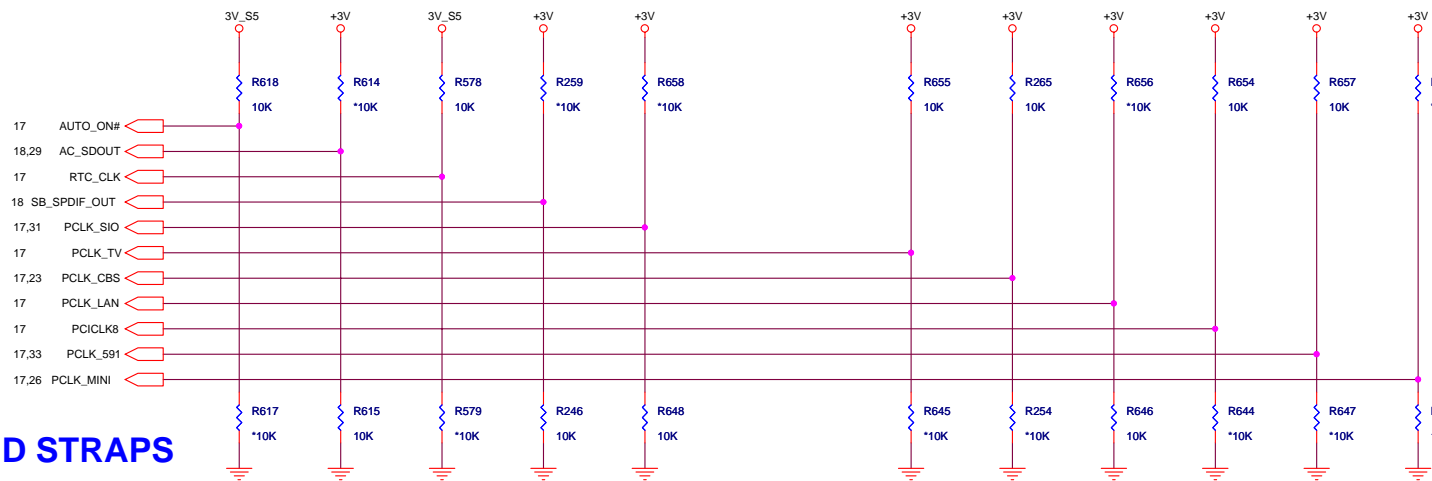




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Quanta Computer Inc.







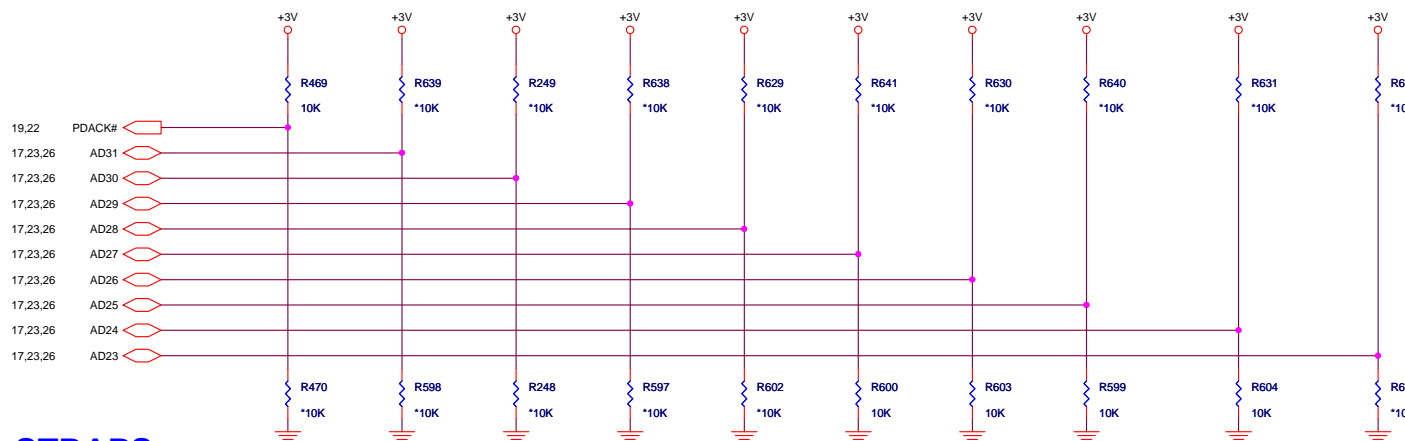
REQUIRED STRAPS

	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCLK_SIO	PCLK_TV	PCLK_CBS	PCLK_LAN	PCI_CLK8	PCLK_591	PCLK_MINI
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz use Internal PLL DEFAULT	14MHz OSC MODE DEFAULT	CPU I/F = K8 DEFAULT	H,H = PCI(X BUS) ROM H,L = LPC ROM I (LPC addresses are translated to the top of the 4G address space) L,H = LPC ROM II DEFAULT (addresses mapped to below 1M) L,L = FWH ROM		USB PHY PWRDOWN DISABLE DEFAULT	48MHz OSC/Clock Buffer
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/IT8712)	SIO 48MHz DEFAULT	48MHz use External Clock	14MHz XTAL MODE	CPU I/F = P4			USB PHY PWRDOWN ENABLE	48MHz Crystal Pad

This strap is only required if the strap on PCICLK4 is configured for External Clock.

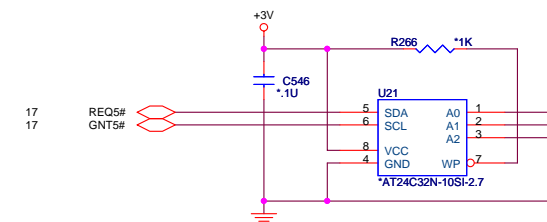


OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



DEBUG STRAPS

	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	



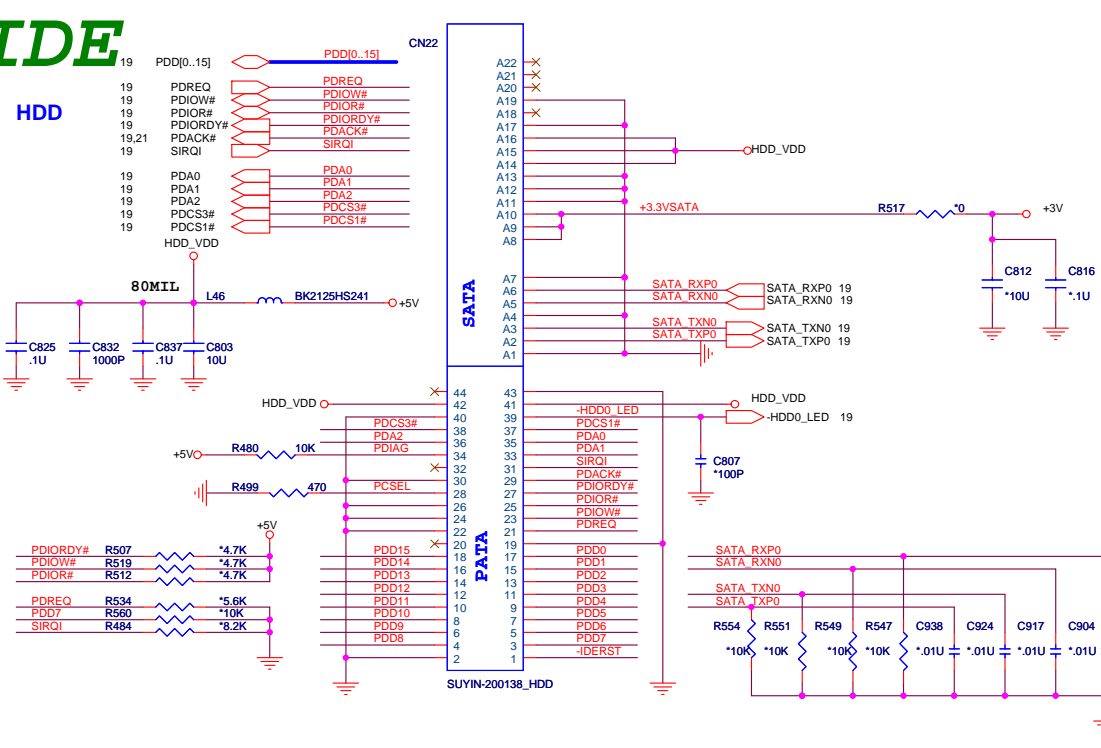
SB PCIE EEPROM STRAPS



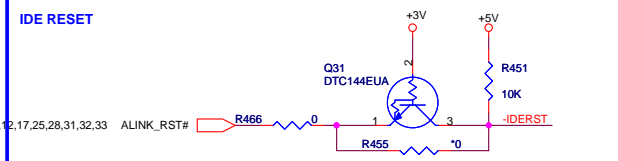
PROJECT : ZF3  
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IDE

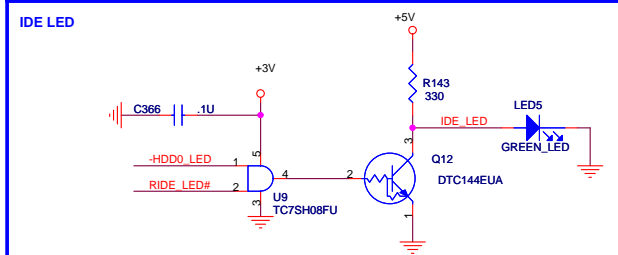
HDD



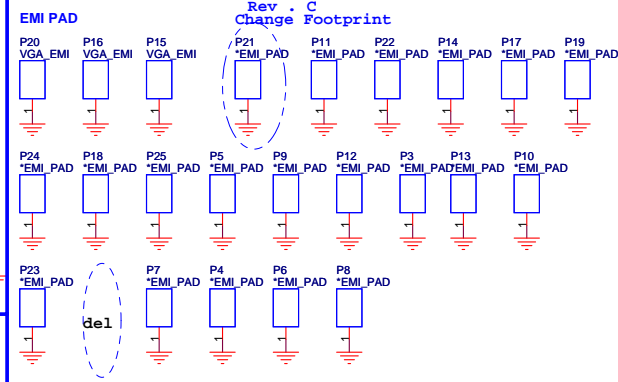
IDE RESET



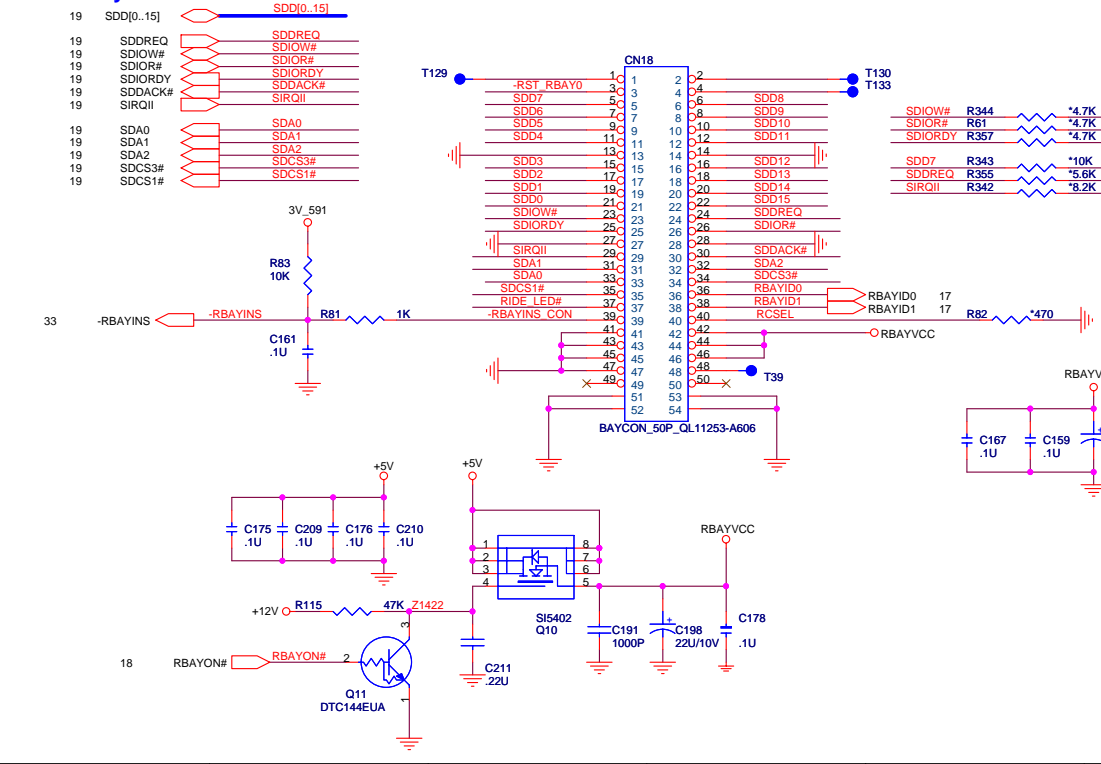
IDE LED



EMI PAD



Multi-Bay Connector



BAY ID STATUS

RBAYID0/ LBAYID0	RBAYID1/ LBAYID1	STATUS
0	1	HDD
1	0	CD/DVD

